Application No. 10/042,358

Please substitute the following amended paragraph for the pending paragraph on page 28, beginning on line 16:

B'

--Figure 3 schematically illustrates a further TFT configuration 50 comprised of a heavily n-doped silicon wafer 56, which can act as a gate electrode, a thermally grown silicon oxide dielectric layer 54, the polythiophene semiconductor layer 52, on top of which are deposited a source electrode 60 and a drain electrode 62. --